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## APPLICATION FOR LETTERS PATENT

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Methods of Forming Semiconductor Circuitry, and  
Semiconductor Constructions

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INVENTORS

Fernando Gonzalez  
Er-Xuan Ping

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**Methods of Forming Semiconductor Circuitry, and Semiconductor**  
**Constructions**

TECHNICAL FIELD

**[0001]** The invention pertains to methods of forming semiconductor circuitry, and in particular applications encompasses methods wherein a mixed semiconductive material substrate is formed. One portion of the mixed semiconductive material substrate can comprise, for example, monocrystalline silicon, and another portion can comprise a semiconductive material that includes at least one atomic percent of an element other than silicon. The invention also pertains to semiconductor constructions.

BACKGROUND OF THE INVENTION

**[0002]** Integrated circuit constructions typically comprise a semiconductive material substrate having circuitry formed thereover. The circuitry can fall within different classes of circuit types, with one exemplary class being memory devices, and another exemplary class being logic devices. For instance, memory chips will frequently comprise an array of memory devices, and will further comprise logic devices peripheral to the memory array. Exemplary memory devices are dynamic random access memory (DRAM) devices.

**[0003]** The memory devices and logic devices can have different desired operating parameters relative to one another. For instance, a highly desired aspect of memory devices can be that such devices have very low off current. In other words it can be desired that very little, if any, current trickle through the devices in an off state. In contrast, peripheral devices can frequently tolerate a

higher off current than memory devices, but it can be desired that the peripheral devices have enhanced mobility of charge within semiconductive substrates incorporated into the devices.

**[0004]** It can be difficult to incorporate memory devices and logic devices into a single integrated circuit while optimizing performance parameters of both the memory devices and logic devices. It would therefore be desirable to develop new methods of forming semiconductor circuitry which could enable optimization of memory device parameters and logic device parameters when the memory devices and logic devices are incorporated into a common integrated circuit construction.

## SUMMARY OF THE INVENTION

**[0005]** In one aspect, the invention encompasses a method of forming semiconductor circuitry. A monocrystalline silicon substrate is provided, and a mask is formed which covers a first portion of the substrate and leaves a second portion uncovered. A trench is formed in the uncovered portion and at least partially filled with a semiconductive material that comprises at least one atomic percent of an element other than silicon. The mask is removed and a first semiconductor circuit component is formed over the first portion of the substrate. Also, a second semiconductor circuit component is formed over the semiconductive material that at least partially fills the trench.

**[0006]** In another aspect, the invention encompasses a semiconductor construction. The construction includes a bulk semiconductive material structure, and an insulative material over the bulk semiconductive material structure. A mass of semiconductive material is over a first portion of the

insulative material and not over a second portion of the insulative material. The semiconductive material of the mass comprises at least one atomic percent of an element other than silicon. A monocrystalline silicon layer is formed over the second portion of the insulative material.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0007]** Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

**[0008]** Fig. 1 is a diagrammatic, cross-sectional, fragmentary view of a semiconductor construction shown at a preliminary processing step of a method of the present invention.

**[0009]** Fig. 2 is a view of the Fig. 1 fragment shown at a processing step subsequent to that of Fig. 1.

**[0010]** Fig. 3 is a view of the Fig. 1 fragment shown at a processing step subsequent to that of Fig. 2.

**[0011]** Fig. 4 is a view of the Fig. 1 fragment shown at a processing step subsequent to that of Fig. 3.

**[0012]** Fig. 5 is a view of the Fig. 1 fragment shown at a processing step subsequent to that of Fig. 4.

**[0013]** Fig. 6 is a view of the Fig. 1 fragment shown at a processing step subsequent to that of Fig. 5.

**[0014]** Fig. 7 is a view of the Fig. 1 fragment shown at a processing step subsequent to that of Fig. 6.

**[0015]** Fig. 8 is a top view of a semiconductor construction illustrating a zoning aspect of the present invention.

**[0016]** Fig. 9 is a diagrammatic, cross-sectional, fragmentary view of a semiconductor construction at a preliminary processing step of a second embodiment method of the present invention.

**[0017]** Fig. 10 is a view of the Fig. 9 fragment shown at a processing step subsequent to that of Fig. 9.

**[0018]** Fig. 11 is a view of the Fig. 9 fragment shown at a processing step subsequent to that of Fig. 10.

**[0019]** Fig. 12 is a view of the Fig. 9 fragment shown at a processing step subsequent to that of Fig. 11.

**[0020]** Fig. 13 is a view of the Fig. 9 fragment shown at a processing step subsequent to that of Fig. 12.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0021]** A first embodiment of the present invention is described with reference to Figs. 1-7. Referring initially to Fig. 1, a semiconductor construction 10 comprises a substrate 12 having an insulative material 14 thereover. Substrate 12 can comprise semiconductive material and can be referred to as a semiconductor substrate. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to,

the semiconductive substrates described above. Monocrystalline material 12 can comprise, consist essentially of, or consist of, silicon.

**[0022]** Insulative material 14 can comprise, for example, silicon dioxide. In particular embodiments, insulative material 14 can consist essentially of, or consist of, silicon dioxide.

**[0023]** A monocrystalline semiconductive material layer 16 is over insulative material 14. Monocrystalline material 16 can comprise, consist essentially of, or consist of, silicon; or can comprise, consist essentially of, or consist of, doped silicon. The construction 10 can be referred to as a silicon on insulator assembly.

**[0024]** The construction of Fig. 1 can be formed by numerous methods. For instance, the construction of Fig. 1 can be formed by providing a single bulk monocrystalline material and subsequently implanting oxide into the material to form the layer 14. The implanted layer 14 separates the initial bulk monocrystalline material into regions 12 and 16 which are spaced from one another by the implanted oxide region 14. Another exemplary process for forming the construction of Fig. 1 is to provide a first substrate which comprises monocrystalline material 12 and a portion of oxide layer 14, and to provide a second substrate which comprises monocrystalline material 16 and another portion of oxide layer 14. The first and second substrates can then be joined to one another by annealing the portion of oxide layer 14 from the first substrate to the portion of oxide layer 14 of the second substrate. Further, the second substrate can have a damage region therein, which is subsequently broken to form layer 16 to a desired thickness. The utilization of a damage region to form

a monocrystalline material to a desired thickness is frequently referred to as "smart cut" technology.

**[0025]** Although the shown embodiment has a first monocrystalline material 12 spaced from a second monocrystalline material 16 by insulative layer 14, it is to be understood that other materials could be provided between monocrystalline materials 12 and 16 in addition to insulative material 14. Accordingly it can be preferred that monocrystalline materials 12 and 16 are spaced from one another by at least insulative material 14, but not necessarily by only insulative material 14. Also, it is to be understood that the invention encompasses embodiments wherein monocrystalline materials 12 and 16 are spaced from one another by an electrically conductive material in addition to, or alternatively to, electrically insulative material 14.

**[0026]** Referring to Fig. 2, a mask 18 is formed over a first segment 20 of monocrystalline material 16, while leaving another segment 22 of monocrystalline material 16 uncovered. In the shown embodiment, mask 18 comprises a first portion 24 of silicon dioxide, and a second portion 26 of silicon nitride. In particular embodiments, layer 26 can consist essentially of, or consist of, silicon nitride; and layer 24 can consist essentially of, or consist of, silicon dioxide.

**[0027]** Silicon dioxide portion 24 is provided as a pad to alleviate stress which could otherwise be formed between silicon nitride layer 26 and monocrystalline semiconductive material 22. Mask 18 can be formed by, for example, photolithographic processing. Specifically, materials 24 and 26 can be initially formed over an entirety of semiconductive material 16, and subsequently a patterned photoresist material (not shown) can be formed over a portion of mask

18 with photolithographic methods. Subsequently, an uncovered portion of mask 18 can be removed with suitable etching. The photoresist can then be stripped to leave the resulting mask structure shown in Fig. 2.

**[0028]** Referring to Fig. 3, semiconductive material 16 is exposed to a suitable etch to form a recess 28 in the uncovered portion 22 of material 16. During such etch, mask 18 protects the covered portion 20 of monocrystalline material 16 from being removed. If monocrystalline material 16 comprises silicon, a suitable etch can be an anisotropic etch comprising one or more of  $\text{CF}_4$ ,  $\text{CF}_3$ ,  $\text{Cl}$ ,  $\text{SF}_6$ ,  $\text{Cl}_2$ , and  $\text{O}_2$ . In the shown embodiment, recess 28 extends only partially into semiconductive material 16, and accordingly does not expose the electrically insulative material 14 underlying semiconductive material 16. It is to be understood, however, that the invention encompasses other embodiments (not shown) wherein the etch removes an entirety of the uncovered portion 22 of semiconductor material 16, and accordingly exposes an upper surface of electrically insulative material 14. Further, the invention encompasses applications in which the etch removes an entirety of the uncovered portion 22 of semiconductor material 16, and penetrates through insulative material 14 to expose an upper surface of semiconductive material 12. It can be preferred to have a bottom portion of recess 28 comprising silicon in applications in which it is ultimately desired to form silicon/germanium within the recess. Recess 28 can have a configuration of, for example, a trench.

**[0029]** Fig. 3 illustrates an optional spacer 29 formed along a sidewall periphery of recess 28. Specifically, spacer 29 is formed along sidewall edges of layers 24 and 26, as well as along an exposed edge of semiconductive material 16 extending within recess 28. Spacer 29 can comprise, consist essentially of,



or consist of, for example, silicon nitride and/or silicon dioxide; and can be formed by deposition of an appropriate material followed by an anisotropic etch of the material.

**[0030]** Referring to Fig. 4, recess 28 is at least partially filled with a material 30 which is preferably a semiconductive material. In the shown embodiment, recess 28 is entirely filled with semiconductive material 30. It is preferred that semiconductive material 30 comprise at least 1% of an element different than that predominantly comprised by semiconductive mass 16. In particular embodiments mass 16 consists essentially of, or consists of, monocrystalline silicon, and it is preferred that semiconductive material 30 comprise at least one atomic percent of an element other than silicon. For instance, semiconductive material 30 can comprise silicon and germanium, with the germanium being present to an atomic concentration of from about 1% to about 20%; can consist essentially of the silicon and germanium; or can consist of the silicon and germanium. In other embodiments, semiconductive material 16 can comprise, consist essentially of, or consist of monocrystalline silicon, and semiconductive material 30 can comprise, consist essentially of, or consist of a III/V compound semiconductive material, such as, for example, Ga/As, Ga/P, In/P, and In/As. In yet other embodiments, mass 30 can comprise, consist essentially of, or consist of, silicon and carbon. An exemplary material which comprises silicon and carbon is silicon carbide. The silicon/carbon material preferably comprises at least about 1 atomic percent carbon.

**[0031]** In a particular embodiment, mass 30 comprises silicon/germanium, and mass 16 comprises monocrystalline silicon. A reason for leaving the shown narrow amount of silicon layer 16 over insulative layer 14 within recess 28 is to

provide a seed layer for subsequent growth of silicon/germanium. The silicon/germanium can be grown as, for example, an epitaxial layer. Exemplary conditions for growing silicon/germanium over a silicon seed layer include a temperature of from about 600°C to about 900°C, a pressure of from about 1 Torr to about 100 Torr, and utilization of one or more of SiH<sub>4</sub>, SiH<sub>2</sub>Cl<sub>2</sub>, HCl, and H<sub>2</sub>.

**[0032]** Referring to Fig. 5, construction 10 is subjected to planarization, such as, for example, chemical-mechanical polishing, to form a planarized upper surface 32 which extends across semiconductive material 30 and layer 26. In particular embodiments, semiconductive material 30 will comprise, consist essentially of, or consist of silicon and germanium, with the germanium being provided to a concentration of from about one atomic percent to about 20 atomic percent. In such embodiments it can be desirable to expose material 30 to an anneal to recrystallize material 30, and thereby improve electron mobility and other physical characteristics of material 30, such as, for example reducing the number of dislocations present within the material. A suitable anneal can be accomplished by exposing material 30 to a temperature of from about 800°C to about 1,100°C for a time of from about 20 seconds to about five minutes, while also exposing material 30 to a laser generating an appropriate wavelength of light so that energy from the laser is absorbed by silicon/germanium material 30. The anneal of material 30 preferably occurs after the planarization of the upper surface of material 30, but can, in other embodiments, occur before such planarization.

**[0033]** Referring to Fig. 6, mask 18 (Fig. 5) is removed. Such removal can be accomplished with an etch selective for the material of mask 18 relative to that of

semiconductive material 30. Alternatively, or in addition, the removal can be accomplished by forming a protective mask (not shown) over material 30 to protect material 30 from etching conditions while exposing the material of mask 18 to an etch which removes mask 18. The etching to remove mask 18 can, as shown, remove at least a portion of spacer 29. In the shown embodiment, the etching has removed only a portion of spacer 29, while leaving another portion to separate a sidewall of material 30 from a sidewall of the material 16 proximate material 30. The shown remaining portion of spacer 29 can advantageously inhibit or prevent lateral exchange of components between materials 16 and 30.

**[0034]** After the removal of mask 18, semiconductive material 30 retains planarized upper surface 32, and semiconductive material 16 has an upper surface 34 which is elevationally below planarized upper surface 32. A distance between upper surface 32 and upper surface 34 is preferably less than or equal to about 200Å so that subsequent photolithographic processing across construction 10 is not adversely impacted by an elevational difference between surfaces 32 and 34. In an exemplary embodiment, an elevational difference between surfaces 32 and 34 is from about 50Å to about 200Å.

**[0035]** The shown construction can be considered to comprise a bulk semiconductive material structure 12 having an insulative material 14 thereover. Mass 30 corresponds to a mass of semiconductor material which is over a first portion of the insulative material and not over a second portion of the insulative material. The monocrystalline material 16 corresponds to a layer which is over the second portion of the insulative material. In the shown embodiment, monocrystalline material 16 further comprises a segment which extends over the first portion of the insulative material, and which is between mass 30 and the first

portion of the insulative material. It is to be understood, however, that the invention encompasses other embodiments (not shown) wherein mass 30 directly physically contacts insulative material 14.

**[0036]** Referring to Fig. 7, a first semiconductor circuit component 36 is formed over surface 34 of monocrystalline semiconductive material 16, and a second semiconductor circuit component 38 is formed over surface 32 of semiconductive material 30.

**[0037]** First semiconductor circuit component 36 comprises a transistor gate, and can comprise, for example, various layers of insulative material, conductively doped silicon, silicide, and/or conductive metal layers, as would be utilized in conventional transistor gate constructions. Sidewall spacers 40 are shown formed along sidewalls of transistor gate 36, and such spacers would typically comprise silicon nitride, silicon dioxide, and/or other electrically insulative materials. An isolation region 42 is shown formed within monocrystalline semiconductive material 16. Isolation region 42 can comprise, for example, silicon dioxide, and can correspond to a shallow trench isolation region. Source/drain regions 44 are shown extending within monocrystalline semiconductor material 16. One of the source/drain regions can be electrically connected to a capacitor construction 46, and the other can be electrically connected to a bit line 48. Accordingly, transistor construction 36 can be incorporated into a DRAM cell.

**[0038]** Transistor gate 38 can comprise similar components as does transistor gate 36, or different components. Transistor gates 36 and 38 will generally comprises stacks of gate oxide (typically silicon dioxide), conductively-doped silicon, and metal silicide. The gate oxide thickness utilized in gate 36

can be different than that utilized in gate 38. Also, the type of conductivity-enhancing dopant utilized in silicon of gate 36 can be different than that utilized in silicon of gate 38.

**[0039]** Sidewall spacers 50 are shown formed along sidewalls of transistor gate 38. An isolation region 52 is shown formed within semiconductor material 30, and such isolation region can correspond to, for example, a shallow trench isolation region. Source/drain regions 54 are shown extending within material 30, and adjacent transistor gate 38. Transistor gate 38 can be incorporated into, for example, logic circuitry.

**[0040]** Fig. 8 is a top view of semiconductor construction 10, and diagrammatically illustrates a zonal configuration of one embodiment of the present invention. The construction of Fig. 8 is shown at a processing step corresponding to that of Fig. 6. Semiconductive material mass 30 extends around an exposed portion 50 of monocrystalline material 16. In other words, upper surface 32 of mass 30 encircles the exposed portion 50 of monocrystalline mass 16. Another exposed portion 52 of mass 16 is shown outwardly of mass 30 relative to the encircled exposed portion 50. The first semiconductor circuit component 36 of Fig. 7 can correspond to a portion of a DRAM array, and such DRAM array can be formed in the encircled portion 50 of monocrystalline mass 16. The second semiconductor circuit component 38 can correspond to a portion of circuitry formed peripheral to the DRAM array, and in the shown embodiment can correspond to a portion of circuitry which encircles the DRAM array. The memory array can be entirely over the exposed portion of monocrystalline material 16, and accordingly not over mass 30. In other words, the invention encompasses embodiments wherein no DRAM cells are formed

over mass 30, but instead an entirety of the DRAM cells of an integrated circuit construction are over the exposed monocrystalline material 16.

**[0041]** A second embodiment of the invention is described with reference to Figs. 9-13. Referring initially to Fig. 9, a semiconductor construction 100 is illustrated at a preliminary processing step. Construction 100 comprises a substrate 102, and a patterned mask 104 over the substrate. Substrate 102 can comprise, for example, a monocrystalline semiconductive material, such as monocrystalline silicon. Mask 104 can comprise a layer 106 of silicon dioxide and a layer 108 of silicon nitride. Mask 104 can be formed utilizing methodology similar to that described above with reference to Fig. 2 for forming mask 18. Mask 104 covers a portion 110 of substrate 102, while leaving another portion 112 not covered.

**[0042]** Referring to Fig. 10, a recess 114 is etched into uncovered portion 112, while mask 104 protects covered portion 110. In embodiments in which substrate 102 comprises monocrystalline silicon, recess 114 can be formed by, for example, etching with one or more of  $\text{CF}_4$ ,  $\text{O}_2$ ,  $\text{CF}_3$ ,  $\text{Cl}$ ,  $\text{SF}_6$ , and  $\text{Cl}_2$ . Recess 114 is preferably formed to a depth of from about 0.1 microns to about 10 microns.

**[0043]** Recess 114 comprises a bottom surface 116 and a sidewall surface 118. In the shown embodiment, an optional spacer 120 is formed across the sidewall surfaces. Spacer 120 can comprise an insulative material 120 such as, for example, silicon dioxide or silicon nitride. In particular embodiments (not shown), spacer 120 can extend across bottom surface 116 of recess 114. Insulative material of spacer 120 can be formed by, for example, deposition of appropriate materials and subsequent etching. Instead of, or in addition to,

deposition, thermal oxidation can be utilized to form material 120 in applications in which material 120 comprises silicon dioxide.

**[0044]** Referring to Fig. 11, a mass 130 of semiconductive material is formed within recess 114. Mass 130 can comprise, for example, the same materials as discussed above with reference to mass 30 of Fig. 4. An advantage of providing spacer 120 is that such can form a barrier between mass 130 and semiconductive material 102 to alleviate or prevent lateral cross-diffusion of components between mass 130 and monocrystalline material 102. It is to be understood, however, that the invention encompasses other embodiments wherein spacer 120 is eliminated. Further, it is to be understood that the invention encompasses embodiments wherein other barrier layers in addition to, or alternatively to, spacer 120 are utilized as a barrier along some or all of an interface between monocrystalline material 102 and semiconductive mass 130.

**[0045]** Referring to Fig. 12, construction 100 is subjected to planarization, such as, for example, chemical-mechanical polishing, to form a planarized upper surface 132 which extends across mass 130 and layer 108 of mask 104. Mass 130 can be subjected to annealing, similar to that discussed above with reference to mass 30, either before or after the planarization of an upper surface of mass 130.

**[0046]** Referring to Fig. 13, mask 104 (Fig. 12) is removed to leave an exposed portion 134 of monocrystalline material 102. Exposed portion 134 comprises an uppermost surface of monocrystalline material 102, and such is elevationally below the uppermost surface 132 of mass 130. A difference in elevation between surfaces 132 and 134 is preferably less than 200Å, and can be, for example, from about 50Å to about 200Å for reasons similar to those

discussed with reference to Fig. 6 regarding the difference in elevation between surfaces 32 and 34.

**[0047]** The construction of Fig. 13 can be alternatively described as a monocrystalline bulk substrate 102 having a semiconductive material mass 130 over a first portion 150, and not over a second portion 152. Mass 130 preferably comprises a semiconductive material different from the semiconductive material of monocrystalline bulk substrate 102. More specifically, if monocrystalline bulk substrate 102 consists essentially of a particular element, such as, for example, silicon, semiconductive material 130 will preferably comprise at least one atomic percent of an element different from that of bulk substrate 102.

**[0048]** Further processing can be performed to form semiconductor circuitry over and/or within semiconductive material 130 and monocrystalline material 102, similar to the processing described above with reference to Figs. 7 and 8.

**[0049]** It is noted that it can be advantageous to round the edges and upper corners of masses 30 (Fig. 6) and 130 (Fig. 13) having abrupt ridges occurring in layers (not shown) that are formed to extend across the edges of masses 30 and 130. The edges and upper corners of masses 30 and 130 can be rounded by, for example, oxidation in particular aspects of the present invention which are not shown.

**[0050]** Among the advantages of methodology of the present invention relative to prior art methodology is that the invention can allow improved speed of DRAM and logic circuit constructions. For example, the present invention can enable improved speed of transistors associated with DRAM circuitry, as well as improved speed of transistors associated with logic circuitry. Specifically the invention can enable the substrate of the peripheral circuitry to be tailored to



meet the needs of the peripheral circuitry, and yet also enable the substrate of the DRAM array circuitry to be tailored to meet the needs of the DRAM circuitry. In particular embodiments, the present invention can enable relatively fast DRAM without sacrificing refresh speed and quality. Additionally, the invention can be incorporated into existing fabrication technologies with relatively little expense.

**[0051]** In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.